WBS 6.8
Trigger

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U.S. ATLAS HL-LHC Upgrade Director's Review
Brookhaven National Laboratory
Upton, New York
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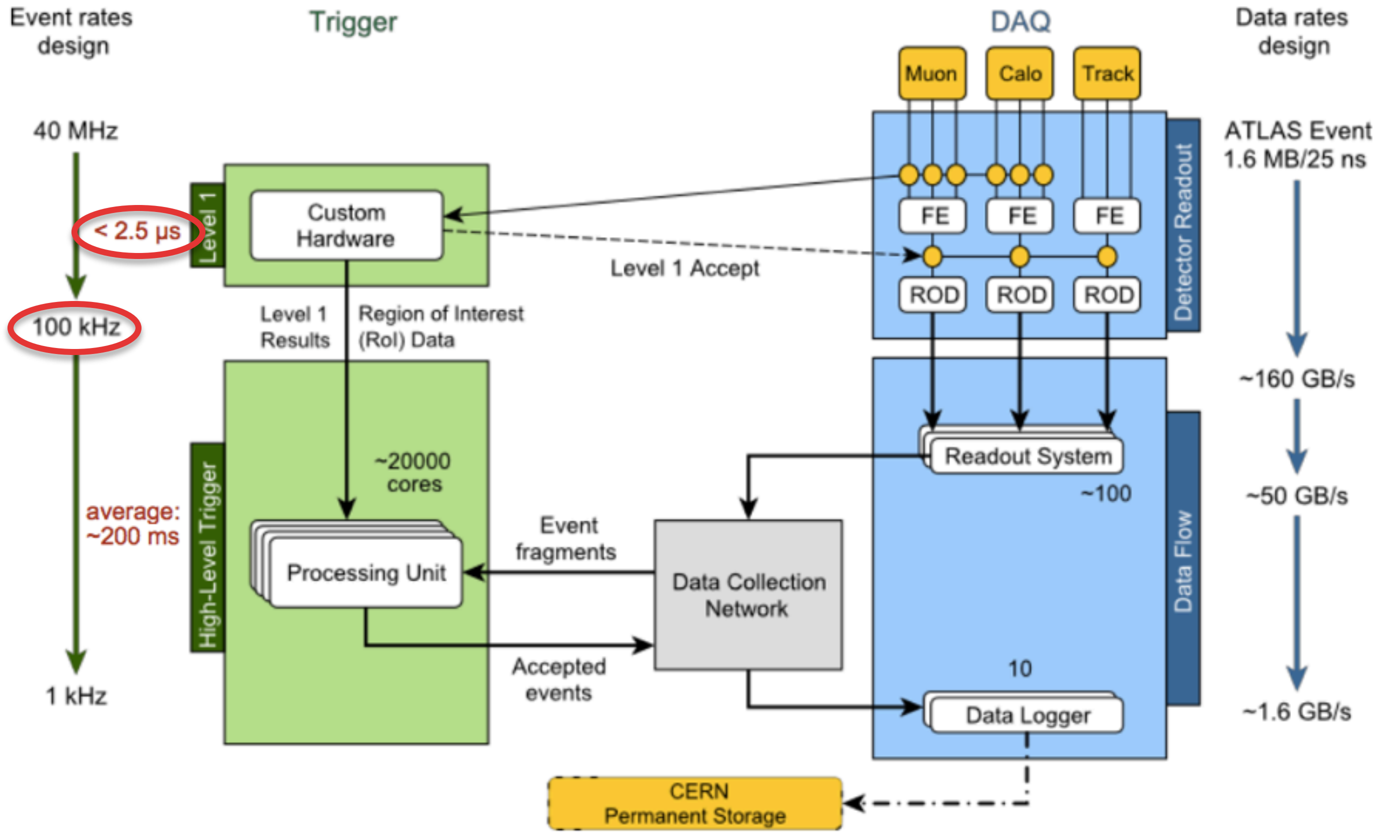
Outline

- System Overview
  - Current (Run-2) System, Phase-1 upgrade and Motivation for Upgrade
  - ATLAS Upgrade Plans
- Proposed U.S. HL-LHC Upgrade Scope
  - Work Breakdown Structure and Contributing Institutes
  - U.S. Deliverables
- Ongoing R&D
  - Plans to Construction Project
  - Funding Needed
- Construction Project Management
  - Construction Project Budget and Schedule
  - Risk, Contingency, and Quality Assurance
- Closing Remarks

Current System

L1 Latency

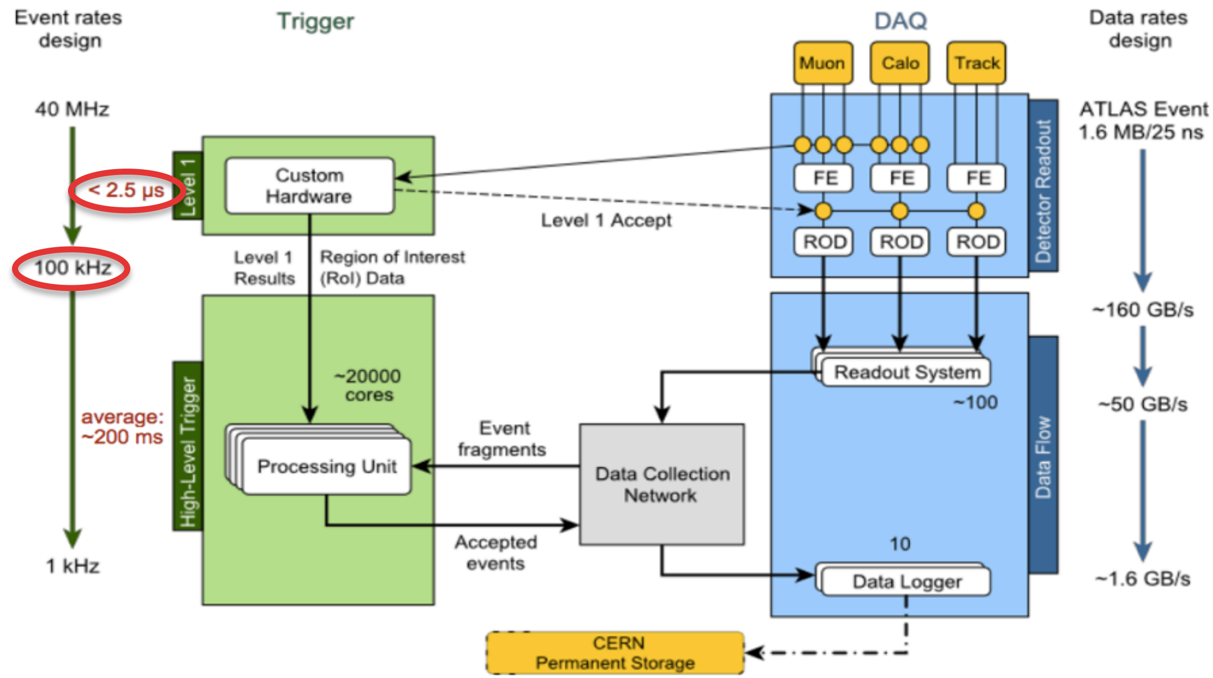
L1 Rate



- Calo = 0.1x0.1 for egamma and 0.2x0.2 for jets
- Muon = only RPC and TGC (fast detectors)
- Tracking only at High-Level Trigger (HLT)

Phase-1 Upgrade

L1 Latency and rate unchanged



- Calo :
  - finer granularity for egamma and jets
  - Added course granularity fat jets and global objects
- Muon: “New small wheel” improves fake rejection for in endcap
- Fast tracking in HLT (full detector at 1 MHz = FTK)

Motivation for HL-LHC Upgrade

General Physics Goal: Maintain Thresholds Close to Run 1

- This is a menu that is proven to support a broad physics program

Rates for ≈Run 1 menu if Phase-1 hardware is not upgraded for Phase-2

Item	Run 1 Offline p_T Threshold [GeV]	Phase-I Level-1 system performance at $L = 7.5 \times 10^{34}\text{cm}^{-2}\text{s}^{-1}$ Offline Threshold for Phase-II Goal [GeV]	Level-1 Rate [kHz]
isolated Single e	25	22	200
single μ	25	20	40
di-γ	25	25	8
di-e	17	15	90
di-μ	12	11	10
$e-\mu$	17,6	17,12	8
single τ	100	150	20
di-τ	40,30	40,30	200
single jet	200	180	60
four-jet	55	75	50
E_T^{miss}	120	200	50
jet + E_T^{miss}	150,120	140,125	60

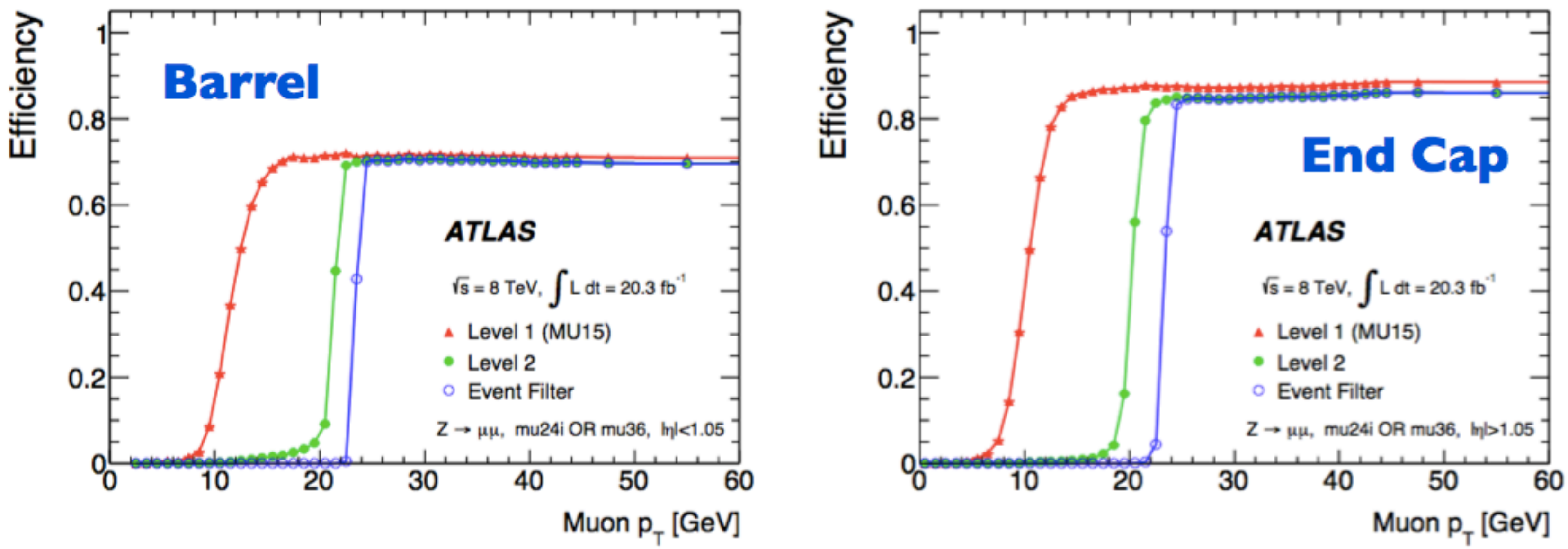
Many triggers in excess of 100 KHz!

Including key single electron trigger

Hadronic triggers allowed to degrade somewhat ("acceptable")

Motivation for HL-LHC Upgrade

Muon efficiency is relatively low in the barrel



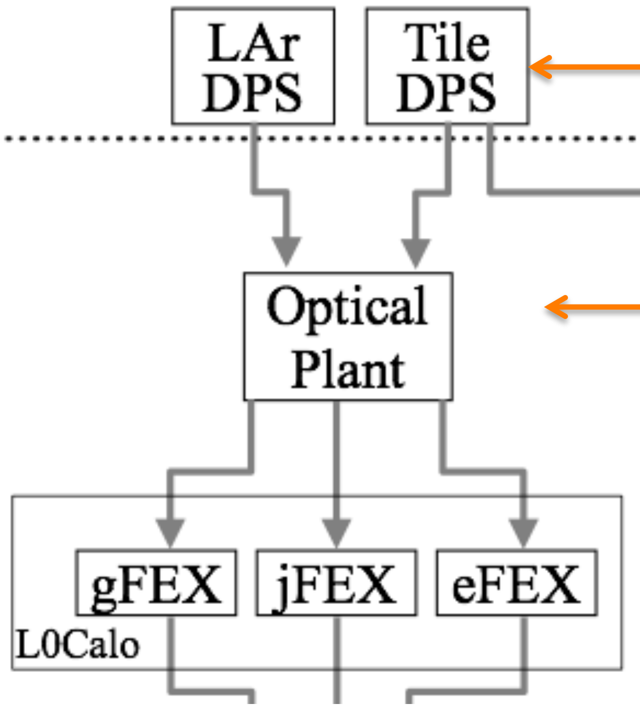
Because the RPC chambers will need to be run at a reduced voltage to avoid aging problems, the effective barrel efficiency would be further reduced to 65%.

- Bad to single muon trigger
- For dimuon triggers, this is a big hit

Motivation for HL-LHC Upgrade

- Trigger inputs must be compatible with planned changes to other systems
  - Tile electronics replacement forces a change in the Calo trigger

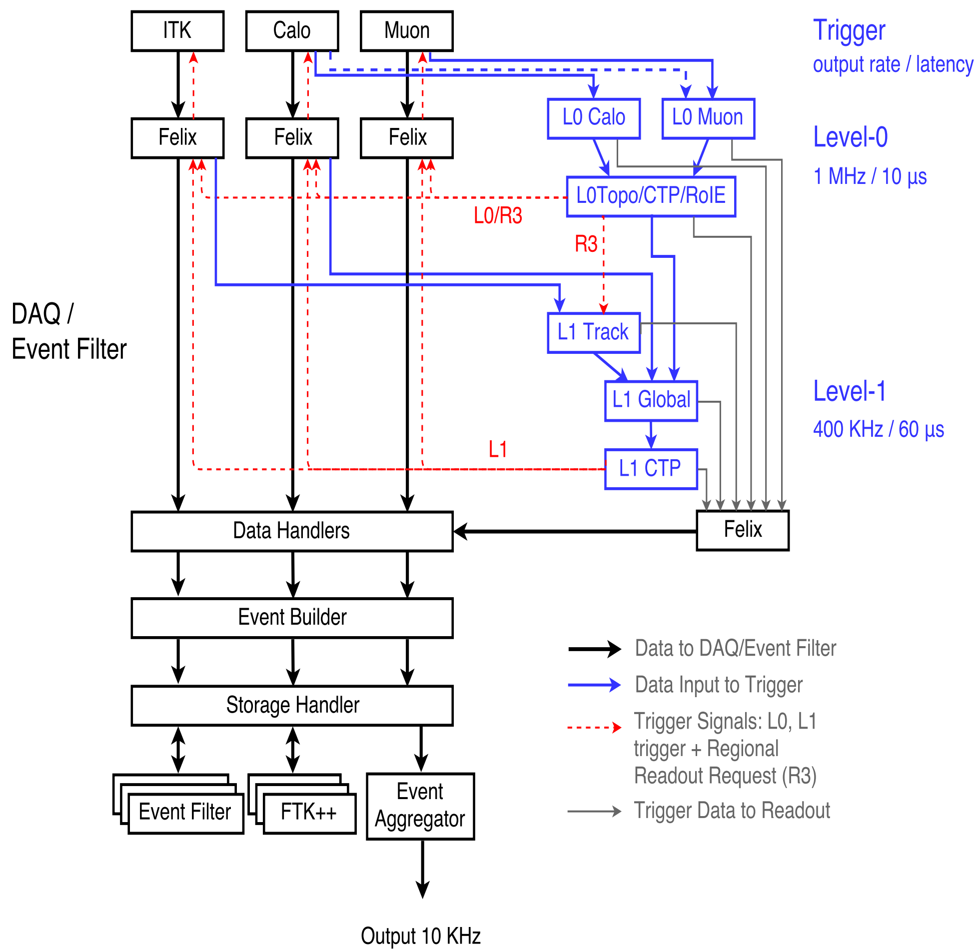
Phase-1 diagram



This is being replaced

so the optical plant needs to change

HL-LHC System Upgrade Plans



Two-level system

- Phase-1 L1 system becomes HL-LHC L0 system
- High precision Muons (MDT) added to L0 system → improves efficiency
- L0 Rate is now 1 MHz
    - Allows in more physics
- L1 system uses tracks and full granularity calo in regions of interest to improve reject before HLT
    - Tracking 10% of data at 1 MHz
- Full detector tracking for 100 KHz events in HLT → mitigates pile-up for hadronic triggers

HL-LHC System Upgrade Performance

Item	Offline p_T Threshold [GeV]	Offline $\|\eta\|$	L0 Rate [kHz]	L1 Rate [kHz]	EF Rate [kHz]
isolated Single e	22	< 2.5	200	40	2.20
forward e	35	$2.4 - 4.0$	40	8	0.23
single γ	120	< 2.4	66	33	0.27
single μ	20	< 2.4	40	40	2.20
di-γ	25	< 2.4	8	4	0.18
di-e	15	< 2.5	90	10	0.08
di-μ	11	< 2.4	20	20	0.25
$e - \mu$	15	< 2.4	65	10	0.08
single τ	150	< 2.5	20	10	0.13
di-τ	40,30	< 2.5	200	30	0.08
single jet	180	< 3.2	60	30	0.60^*
fat jet	375	< 3.2	35	20	0.35^*
four-jet	75	< 3.2	50	25	0.50^*
H_T	500	< 3.2	60	30	0.60^*
E_T^{miss}	200	< 4.9	50	25	0.50^*
jet + E_T^{miss}	140,125	< 4.9	60	30	0.30^*
forward jet**	180	3.2 - 4.9	30	15	0.30^*
Total			~1000	~400	~10

- Resulting menu is comparable to the Run 1 menu

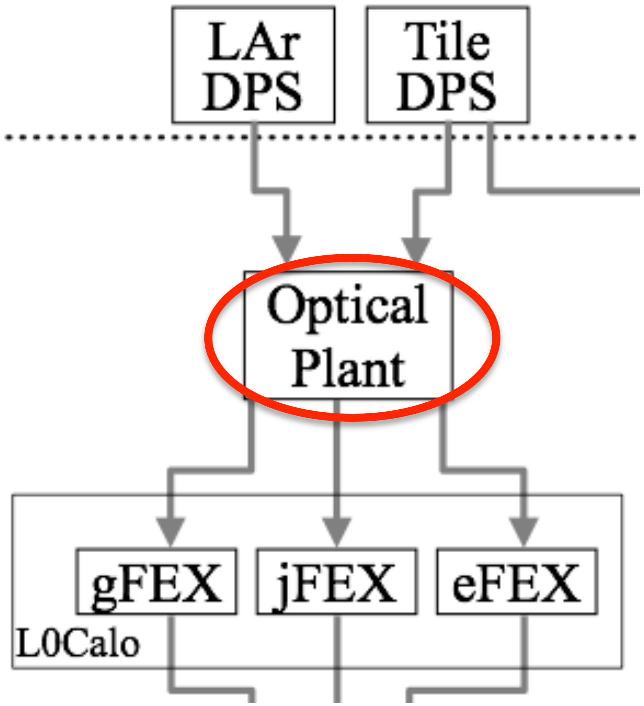
Proposed U.S. Scope

WBS #	WBS Title	WBS Dictionary	Collaborating Institution
6.8.y.1	L0 Calo	Design and build the Fiber Input/Output system for the Tile Calorimeter inputs to the HL-LHC L0 Calorimeter FEX systems. This will be an optical fiber plant consisting of splitters and connectors. Institutes = MSU	MSU
6.8.y.2	L0 Muon	The MDT information will be included in the L0 Muon trigger for the HL-LHC system. This system will process the MDT hits stream at the full 40 MHz beam crossing rate. This package is for 32 FPGA-based Advanced Mezzanine Cards and associated firmware which to perform the track segment finding, segments linking and the track fitting.	Irvine
6.8.y.3	L1 Global Firmware	L1Global hadronic triggering firmware, includes algorithm implementation for topological clustering, jet finding, fat-jet identification, global quantity reconstruction, and the use of tracking information in pile-up rejection.	Chicago Indiana LTU MSU Oregon Pitt
6.8.y.4	L1 Track/FTK++ Processing	The L1Track and FTK++ systems will provide hardware-based tracking for the HL-LHC ATLAS trigger. The L1Track system will operate at 1 MHz in regions of interest totaling 10% of the event giving a result with a latency < 20 microseconds, so that it can be used in the L1 decision. FTK++ will provide full detector tracking for 100 kHz of events to be used in the Event Filter (no significant latency constraint). The system is divided in to two stages which use a common mainboard for data formatting and system interface. The second stage is a track-fitting stage. This package consists of 690 mainboards and 1104 track-fitting mezzanines for low-latency regional at tracking 1 MHz and 100 kHz of full detector tracking	Indiana Penn Chicago Illinois NIU Stanford

- General scope has been discussed with ATLAS TDAQ management, but they are not ready to make commitments

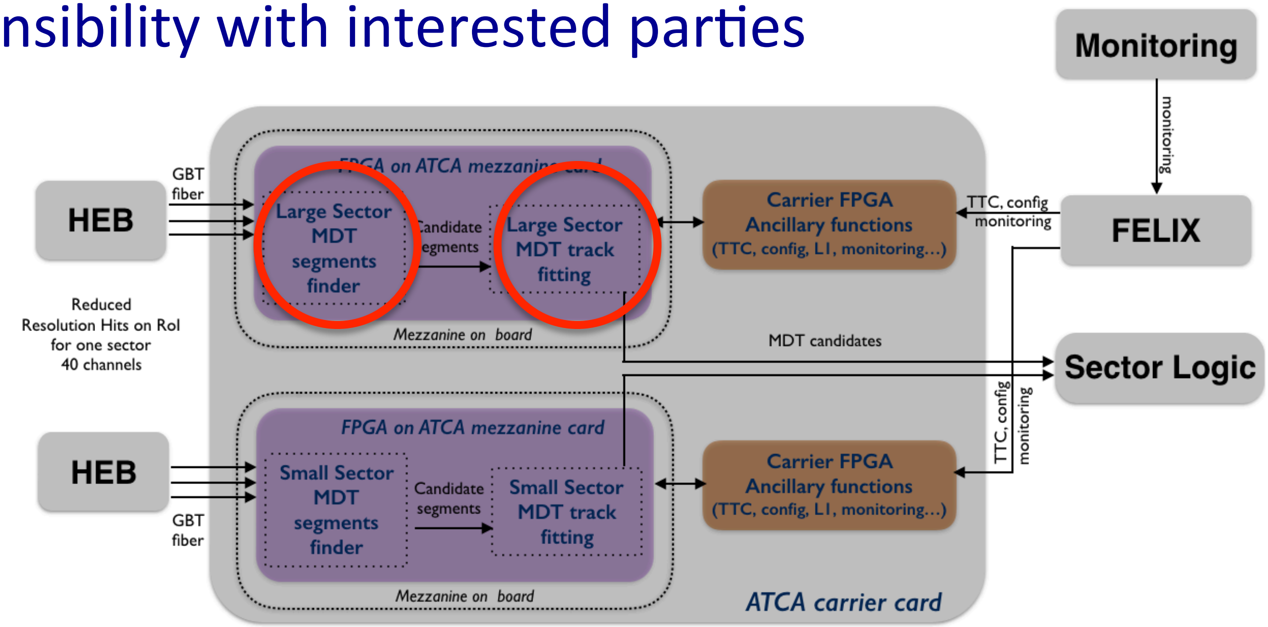
6.8.y.1: L0 Calo Fiber Optic Plant

- This is a minor change to the existing Fiber Optic plant to accommodate the change to the tile electronics
- This is agreed to be US deliverable as was the original system



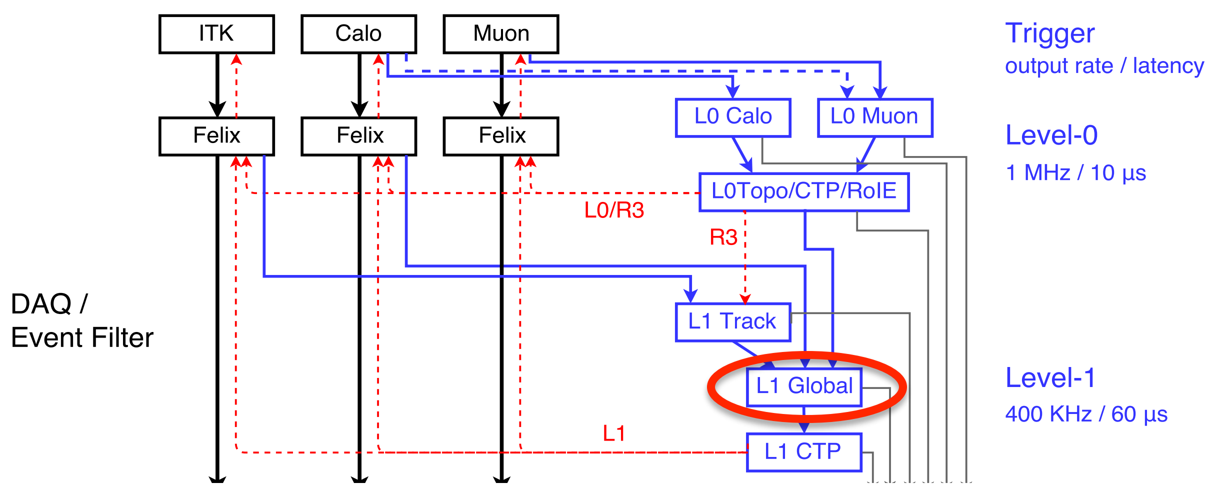
6.8.y.2: L0 Muon

- Deliverable is a mezzanine card with firmware that sits on a carrier card that handles the I/O with the system
  - Mezzanine find track segments, links them, and fits tracks
- Scope is consistent with a preliminary discussion of US responsibility with interested parties



6.8.y.3: L1 Global Processing

- Deliverable is firmware that runs on the L1 Global Processor
  - The focus is on hadronic triggering with 4 related items
    - Offline-like "topological clustering" of calorimeter energy
    - Offline-like jet finding
    - Global quantities: Missing energy, sum of jet pTs (HT), and MHT
    - Track-based pile-up rejection for multijet and global quantities
- Scope of firmware has been discussed with and encouraged by TDAQ management



6.8.y.4: L1Track/FTK++ processing

- The L1Track/FTK++ systems are expected to use the same hardware with minor modifications
- Each system consists of two stages:
  - pattern recognition step with a preliminary track fit
  - second track fitting stage to include additional hits not used in pattern rec
- Both stages are expect to use the same mainboard for data preparation
- Each stage will have its own mezzanine
- Proposed deliverables are
  - Mainboard design and firmware (50% of hardware)
  - 100% Second-stage hardware and firmware
- Scope amounts to ~50% of total project which is consistent with a discussion with TDAQ management

Research & Development

- 6.8.y.1 L0 Calo
  - Fiber plant is similar enough to Phase-1 that no early R&D is needed
- 6.8.y.2 L0 Muon to start in FY17
  - Preliminary algorithm with timing in FPGA, latency estimate for TDR (end-2017)
  - Later R&D for first prototype board
- 6.8.y.3 L1 Global processing
  - has begun to better understand how to implement iterative cluster finding in FPGAs, will give input on processor selection
- 6.8.y.4 L1Track/FTK++
  - Starting in FY18, mainboard studies include barebones test board for full mesh ATCA interaction
  - Starting in FY18, mezzanine prototype board to test FPGA to memory speeds (give input to FPGA/memory selection)

	FY17	FY18	FY19	FY20	TOTAL
Total	**219.7**	**390.2**	**366.6**	**461.3**	**1,437.9**
Labor (Ayk$)	175.03	314.44	293.30	419.72	1,202.49
M&S (Ayk$)	35.35	50.51	47.80	17.00	150.65
Labor (Ayk$)	9.36	25.24	25.53	24.61	84.73
FTE – Total	**1.05**	**1.75**	**1.50**	**2.25**	**6.55**

Schedule

Will we instead have a plot from the project office?

Milestones

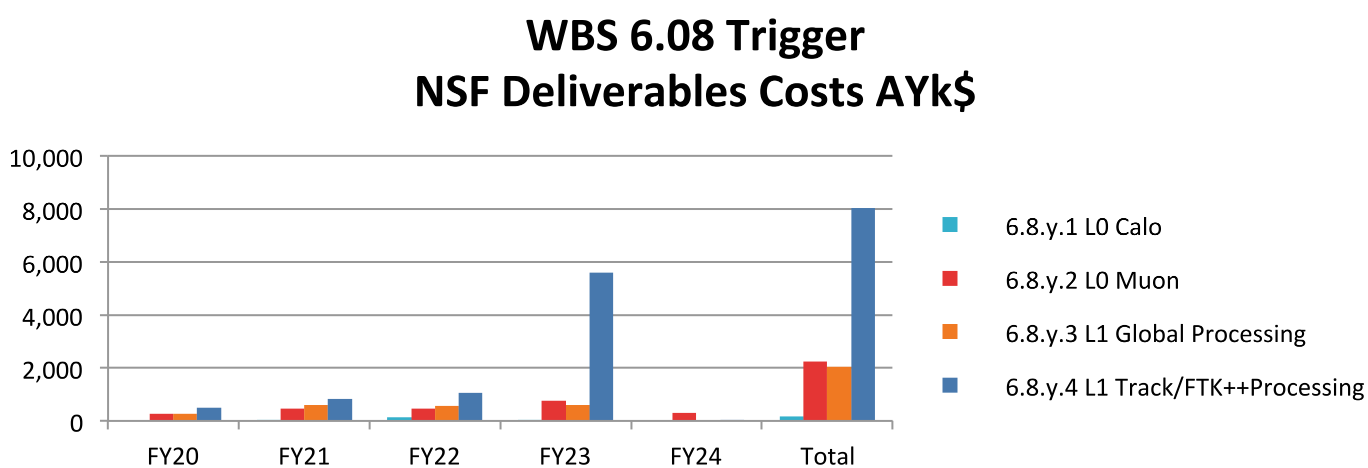
- R&D Milestones:
  - MDT latency estimates end-2017
- Reviews: dates for IDR, TDR, FDR(s)
  - TDAQ IDR will be reviewed early 2016
  - TDAQ TDR is scheduled for end-2017
  - FDR varies by component:
    - L0 Calo Q2 2020
    - L0 Muon Q4 2021
    - L1 Global Q4 2020
    - L1Track/FTK++ Q4 2020

Cost and Effort Estimates

- 6.8.y.1 L0 Calo
  - Based on Phase-1 fiber plant
- 6.8.y.2 L0 Muon
  - MDT mezzanine based on experience with Phase-1 NSW and expert opinion using one possible system configuration
- 6.8.y.3 L1 Global Processing
  - Per algorithm effort based on Phase-1 gFEX algorithm work and expert opinion for differences
- 6.8.y.4 L1Track/FTK++
  - Based on FTK++ experience and numerical estimates of the data volume and number of patterns needs using ATLAS work from scoping document

Budget Summary

6.08 Trigger NSF Total Cost (AYk$)						
Item/Phase	**FY20**	**FY21**	**FY22**	**FY23**	**FY24**	**Total**
6.8.y.1 L0 Calo	0	43	126	19	0	187
6.8.y.2 L0 Muon	265	456	466	778	291	2,256
6.8.y.3 L1 Global Processing	269	611	569	586	0	2,035
6.8.y.4 L1 Track/FTK++Processing	494	835	1,054	5,598	51	8,032
Main Board	247	417	628	3,479	0	4,771
Mezzanine	247	417	427	2,119	51	3,261
NSF Grand Total	1,029	1,943	2,215	6,980	343	12,510



Budget Summary

6.08 Trigger NSF Total Cost (AYk$)						
Item/Phase	**FY20**	**FY21**	**FY22**	**FY23**	**FY24**	**Total**
6.8.y.1 L0 Calo	**0**	**43**	**126**	**19**	**0**	**187**
Design	0	43	0	0	0	43
Prototype	0	0	0	0	0	0
Pre-production	0	0	0	0	0	0
Production	0	0	126	19	0	144
6.8.y.2 L0 Muon	**265**	**456**	**466**	**778**	**291**	**2,256**
Design & Prototype	265	362	0	0	0	627
Pre-production	0	94	466	0	0	560
Production	0	0	0	778	291	1,069
6.8.y.3 L1 Global Processing	**269**	**611**	**569**	**586**	**0**	**2,035**
Design	0	0	0	0	0	0
Prototype	269	0	0	0	0	269
Pre-production	0	611	0	0	0	611
Production	0	0	569	586	0	1,155
6.8.y.4 L1 Track/FTK++Processing	**494**	**835**	**1,054**	**5,598**	**51**	**8,032**
Main Board	**247**	**417**	**628**	**3,479**	**0**	**4,771**
Design	0	0	0	0	0	0
Prototype	247	417	0	0	0	664
Pre-production	0	0	628	0	0	628
Production	0	0	0	3,479	0	3,479
Mezzanine	**247**	**417**	**427**	**2,119**	**51**	**3,261**
Design	0	0	0	0	0	0
Prototype	247	417	0	0	0	664
Pre-production	0	0	427	0	0	427
Production	0	0	0	2,119	51	2,170
NSF Grand Total	**1,029**	**1,943**	**2,215**	**6,980**	**343**	**12,510**

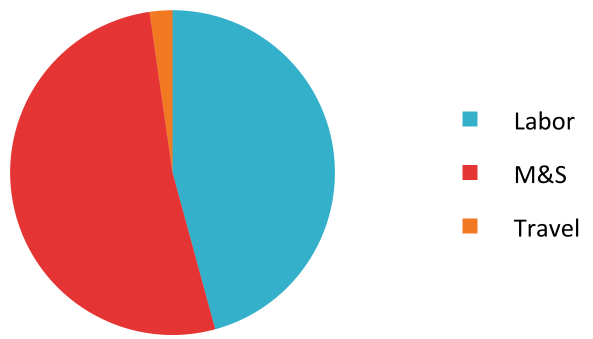
Effort Details

6.08 Trigger NSF FTEs by Labor Types						
Item/Phase	**FY20**	**FY21**	**FY22**	**FY23**	**FY24**	**Total**
6.8.y.1 L0 Calo	**-**	**0.25**	**0.42**	**0.08**	**-**	**0.75**
Engineer	-	0.25	0.42	0.08	-	0.75
Technician	-	-	-	-	-	-
Student	-	-	-	-	-	-
6.8.y.2 L0 Muon	**1.50**	**2.75**	**2.75**	**2.75**	**2.06**	**11.81**
Engineer	1.00	1.75	1.00	0.75	0.56	5.06
Technician	-	-	0.75	1.00	0.75	2.50
Student	0.50	1.00	1.00	1.00	0.75	4.25
6.8.y.3 L1 Global Processing	**1.25**	**2.50**	**2.50**	**2.50**	**-**	**8.75**
Engineer	1.25	2.50	2.50	2.50	-	8.75
Technician	-	-	-	-	-	-
Student	-	-	-	-	-	-
6.8.y.4 L1 Track/FTK++Processing	**2.50**	**4.00**	**2.00**	**1.75**	**0.25**	**10.50**
Main Board	**1.25**	**2.00**	**1.00**	**1.00**	**-**	**5.25**
Engineer	1.00	1.75	0.75	0.75	-	4.25
Technician	0.25	0.25	0.25	0.25	-	1.00
Student	-	-	-	-	-	-
Mezzanine	**1.25**	**2.00**	**1.00**	**0.75**	**0.25**	**5.25**
Engineer	1.00	1.75	0.75	0.58	0.17	4.25
Technician	0.25	0.25	0.25	0.17	0.08	1.00
Student	-	-	-	-	-	-
NSF Grand Total	**5.25**	**9.50**	**7.67**	**7.08**	**2.31**	**31.81**
Engineer	4.25	8.00	5.42	4.66	0.73	23.06
Technician	0.50	0.50	1.25	1.42	0.83	4.50
Student	0.50	1.00	1.00	1.00	0.75	4.25

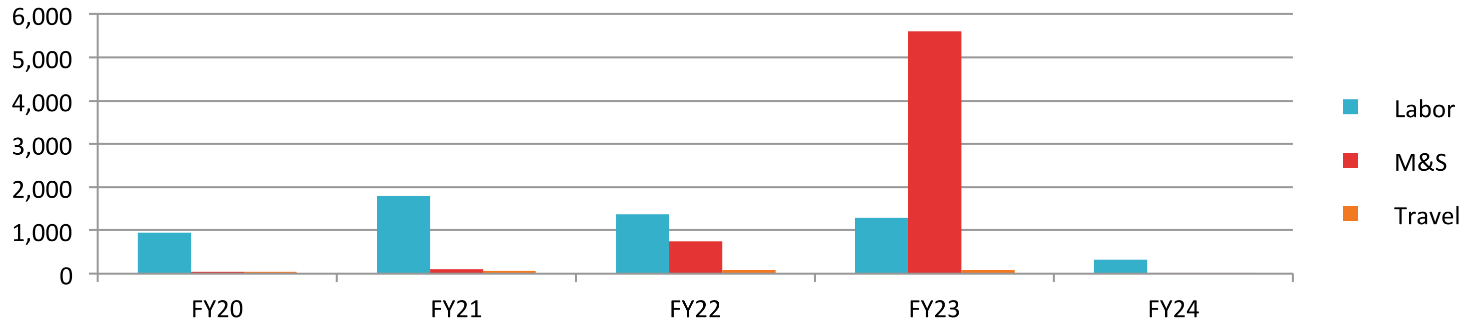
Budget Summary

6.08 Trigger NSF Total Cost (AYk$)						
	FY20	FY21	FY22	FY23	FY24	Grand Total
NSF						
Labor	958	1,786	1,371	1,288	322	5,725
M&S	39	96	753	5,606	9	6,502
Travel	32	61	91	86	12	283
NSF Total	**1,029**	**1,943**	**2,215**	**6,980**	**343**	**12,510**

WBS 6.08 Trigger L2 NSF Resource Breakdown



WBS 6.08 Trigger L2 NSF Fiscal Year Costs AYk$



Off Project Effort

- 6.8.y.1 L0 Calo
  - No significant need
- 6.8.y.2 L0 MDT
  - Once project scientist is phased out in R&D, physicist support will be need for continued algorithm simulation and refinement
- 6.8.y.3 L1 Global Processing
  - It is expected that the algorithms will be developed in conjunction with physicists are each university and implemented in hardware by the requested manpower

Off Project Effort (con't)

- 6.8.y.4 L1Track/FTK++
  - Simulation work for TDR
    - Algorithm simulation for determining how many AM chip patterns are need and how many fits per event are needed are expected to be completed by ATLAS physicists (UK groups have already provide a large part of this for L1Track)
    - Global simulation of the latency chain for L1Track will be provided by ATLAS physicists (needed for the TDR, preliminary work done by UK and Penn)
  - Construction firmware programming
    - Construction budget assumes that graduate students and postdocs will write a large part of the firmware with engineering support from 0.25 FTE/year per item (mainboard, mezzanine)
    - This model is working well for the current FTK development with the very good training experience for those involved

Risks

- 6.8.y.1 L0 Calo
  - The final logical map from the Tile calorimeter to the FEX boards could be delayed.
  - There is sufficient leeway in the schedule to accommodate delays
- 6.8.y.2 L0 Muon
  - R&D does not yield sufficient information to clearly define the specifications of the AMC and firmware
  - Cost of the project is driven by the FPGA cost. Final FPGA cost may be higher than currently estimated.
  - The ATCA carrier card will be developed by international collaborators. Delay in delivery will reduce the testing time of the final integrated MDT trigger processor system

Risks

- 6.8.y.3 L1 Global Processing
  - Production boards are not available until later than expect. Only a large deviation from the schedule would have an impact, so the probability is considered low.
  - Firmware implementation is more complex than initially expected.
  - As the understanding of the pile-up advances, algorithms are more complex than expected. The task up understanding jets in high pile-up is ongoing so innovation is still possible.

- 6.8.y.4 L1Track/FTK++
  - Sufficient student/postdoc effort from base program not available for the firmware development. This is largely a schedule issue because we can expect the contributing instates to have some manpower on an ongoing basis, but maybe not enough to complete the task on schedule.
  - The firmware developed by students is not adequate. Experience with the FTK project suggests that this is unlikely. Some engineering support has been included to mentor the students and help assure the quality of the firmware.
  - AMChip cannot support as many patterns as expected

Contingency

- Schedule Contingency (assume every needed at CERN end CY 24)

Deliverable	Base Budget	Schedule Float
6.8.y.1: L0 Calo	$187k	15 months
6.8.y.2: L0 Muon	$2256k	12 months
6.8.y.3: L1 Global Processing	$2035k	15 months
6.8.y.4: L1Track/FTK++	$8032k	12 months

- Scope Contingency
  - Early = FY20, remove one L1 Global algorithm -$380k
  - Late = FY22, 30% instead of 50% L1Track/FTK++ mainboards $-1140k
    - Either someone else in ATLAS (non-US) will pay or the efficiency/coverage will be reduced
- Scope Opportunity
  - Early = FY20, remove one L1 Global algorithm -$380k

Closing Remarks

- US Deliverables
  - 6.8.y.1 L0 Calo fiber optic plant for new tile output
  - 6.8.y.2 L0 Muon MDT segment finding and fitting mezzanine
  - 6.8.y.3 L1 Global Processing algorithms for hadronic objects
  - 6.8.y.4 L1Track/FTK++ mainboard and second stage fitting mezzanines
- Schedule summary
  - TDAQ TDR end-2017
    - MDT muon needs detailed latency estimate
      - Engineering for algorithm timing, algorithms development and global latency is off-project
    - L1Track/FTK++ needs latency and bandwidth
      - algorithms development and global latency is off-project
  - Proposed production period: FY23 to Q2 FY24
- Total budget for this L2 (no contingency): : $12,510k

Backup

Quality Assurance Plans

Definition of Successful End of Project

- 6.8.y.1 L0 Calo
  - Delivery of assembled and tested system
- 6.8.y.2 L0 Muon
  - Delivery to CERN of 32 AMCs which have been tested with the carrier boards
- 6.8.y.3 L1 Global Processing
  - Completion functional algorithms with adequate demonstrated performance, resource consumption and timing
- 6.8.y.4 L1Track/FTK++
  - Delivery of boards to CERN with firmware that is ready for an full integration test (slice test will be a year early)

Single-Level vs L0/L1 split

- Decision in expected in summer 2016
- There is discussion in ATLAS to consider the possibility of removing the L0/L1 split
- In this scenario the HLT does all the work that the L1 previously did
  - There is still a need for high-rate tracking in hardware
    - relatively small impact on plan
    - L1Track/FTK++ will be reconfigured, but hardware is likely to still exist
  - The L1Global functionality to process high granularity calorimeter information at a high rate is still needed, but it could take a very different form
    - Many options none of which are studied in detail in ATLAS
      - Preprocessing in LAr and Tile preprocessors?
      - GPU/CPU(?) processing in augmented EF farm?
      - Move L1Global to L0Global?